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Inventor Name Search Result

Your Search was:

Last Name = WISOR
First Name = MICHAEL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08650523	5920891	150	05/20/1996	ARCHITECTURE AND METHOD FOR CONTROLLING A CACHE MEMORY	WISOR, MICHAEL
08960819	5964859	150	10/30/1997	ALLOCATABLE POST AND PREFETCH BUFFERS FOR BUS BRIDGES	WISOR, MICHAEL
09135065	6247146	150	08/17/1998	METHOD FOR VERIFYING BRANCH TRACE HISTORY BUFFER INFORMATION	WISOR, MICHAEL
09135493	6173395	150	08/17/1998	MECHANISM TO DETERMINE ACTUAL CODE EXECUTION FLOW IN A COMPUTER	WISOR, MICHAEL
09137572	6430705	150	08/21/1998	METHOD FOR UTILIZING VIRTUAL HARDWARE DESCRIPTIONS TO ALLOW FOR MULTI-PROCESSOR DEBUGGING IN ENVIRONMENTS USING VARYING PROCESSOR REVISION LEVELS	WISOR, MICHAEL
09137610	6128727	250	08/21/1998	SELF MODIFYING CODE TO TEST ALL POSSIBLE ADDRESSING MODES	WISOR, MICHAEL
09639390	6336212	250	08/15/2000	Self modifying code to test all possible addressing modes	WISOR, MICHAEL
08649536	5790871	150	05/17/1996	SYSTEM AND METHOD FOR TESTING AND DEBUGGING A MULTIPROCESSING INTERRUPT CONTROLLER	WISOR, MICHAEL T
10756551	Not Issued	30	01/13/2004	Hardware initialization method that is independent of boot code architecture	WISOR, MICHAEL T.
10968414	Not Issued	61	10/19/2004	Non-volatile memory system having a programmably selectable boot code section size	WISOR, MICHAEL T.
08156888	Not Issued	166	11/23/1993	POWER MANAGEMENT CONTROL TECHNIQUE FOR TIMER TICK ACTIVITY WITHIN AN INTERRUPT DRIVEN COMPUTER SYSTEM	WISOR, MICHAEL T.
08160930	5442794	150	12/01/1993	DISABLE TECHNIQUE EMPLOYED DURING LOW BATTERY	WISOR, MICHAEL T.

				CONDITIONS WITHIN A PORTABLE COMPUTER SYSTEM	
08190279	5504910	150	02/02/1994	POWER MANAGEMENT UNIT INCLUDING SOFTWARE CONFIGURABLE STATE REGISTER AND TIME-OUT COUNTERS FOR PROTECTING AGAINST MISBEHAVED SOFTWARE	WISOR, MICHAEL T.
08190285	5671424	150	02/02/1994	IMMEDIATE SYSTEM MANAGEMENT INTERRUPT SOURCE WITH ASSOCIATED REASON REGISTER	WISOR, MICHAEL T.
08190292	5511203	150	02/02/1994	POWER MANAGEMENT SYSTEM DISTINGUISHING BETWEEN PRIMARY AND SECONDARY SYSTEM ACTIVITY	WISOR, MICHAEL T.
08190597	Not Issued	166	02/02/1994	SYSTEM MANAGEMENT INTERRUPT SOURCE INCLUDING A PROGRAMMABLE COUNTER AND POWER MANAGEMENT SYSTEM EMPLOYING THE SAME	WISOR, MICHAEL T.
08223643	Not Issued	166	04/06/1994	FAIL-SAFE COMMUNICATIONS ABORT MECHANISM FOR PARALLEL PORTS	WISOR, MICHAEL T.
08223770	6021498	150	04/06/1994	POWER MANAGEMENT UNIT INCLUDING A PROGRAMMABLE INDEX REGISTER FOR ACCESSING CONFIGURATION REGISTERS	WISOR, MICHAEL T.
08247092	5422862	150	05/20/1994	COMPUTER SYSTEM EMPLOYING AN IMPROVED REAL TIME CLOCK ALARM	WISOR, MICHAEL T.
08308151	5678065	150	09/19/1994	COMPUTER SYSTEM EMPLOYING AN ENABLE LINE FOR SELECTIVELY ADJUSTING A PERIPHERAL BUS CLOCK FREQENCY	WISOR, MICHAEL T.
08308596	5625807	150	09/19/1994	SYSTEM AND METHOD FOR ENABLING AND DISABLING A CLOCK RUN FUNCTION TO CONTROL A PERIPHERAL BUS CLOCK SIGNAL	WISOR, MICHAEL T.
08410217	5606662	150	03/24/1995	AUTO DRAM PARITY ENABLE/DISABLE MECHANISM	WISOR, MICHAEL T.
08454613	Not Issued	166	05/31/1995	SYSTEM AND METHOD FOR PATCHING MICROCODE DURING THE DEBUGGING OF A PROCESSOR	WISOR, MICHAEL T.
08455508	Not Issued	161	05/31/1995	INTERNAL STATE DUMP MECHANISM FOR SAVING PROCESSOR VALUES DURING SYSTEM TESTING	WISOR, MICHAEL T.
08554396	5606713	150	11/06/1995	SYSTEM MANAGEMENT INTERRUPT	WISOR, MICHAEL T.

				SOURCE INCLUDING A PROGRAMMABLE COUNTER AND POWER MANAGEMENT SYSTEM EMPLOYING THE SAME	
08623020	5790783	150	03/28/1996	METHOD AND APPARATUS FOR UPGRADING THE SOFTWARE LOCK OF MICROPROCESSOR	WISOR, MICHAEL T.
08623021	5790663	150	03/28/1996	METHOD AND APPARATUS FOR SOFTWARE ACCESS TO A MICROPROCESSOR SERIAL NUMBER	WISOR, MICHAEL T.
08623022	5933620	150	03/28/1996	METHOD AND APPARATUS FOR SERIALIZING MICROPROCESSOR IDENTIFICATION NUMBERS	WISOR, MICHAEL T.
08623024	5774544	150	03/28/1996	METHOD AND APPARATUS FOR ENCRYPTING AND DECRYPTING MICROPROCESSOR SERIAL NUMBERS	WISOR, MICHAEL T.
08627878	5768499	150	04/03/1996	METHOD AND APPARATUS FOR DYNAMICALLY DISPLAYING AND CAUSING THE EXECUTION OF SOFTWARE DIAGNOSTIC/TEST PROGRAMS FOR THE SILICON VALIDATION OF MICROPROCESSORS	WISOR, MICHAEL T.
08649537	5799203	150	05/17/1996	A SYSTEM FOR RECEIVING PERIPHERAL DEVICE CAPABILITY INFORMATION AND SELECTIVELY DISABLING CORRESPONDING PROCESSING UNIT FUNCTION WHEN THE DEVICE FAILING TO SUPPORT SUCH FUNCTION	WISOR, MICHAEL T.
08649538	5946497	150	05/17/1996	SYSTEM AND METHOD FOR PROVIDING MICROPROCESSOR SERIALIZATION USING PROGRAMMABLE FUSES	WISOR, MICHAEL T.
08657524	Not Issued	166	06/03/1996	SYSTEM AND METHOD FOR PATCHING MICROCODE DURING THE DEBUGGING OF A PROCESSOR	WISOR, MICHAEL T.
08687901	Not Issued	161	07/29/1996	METHOD TO PROVIDE A CLOCK SPEED LIMITER TO SET MAXIMUM PROCESSOR CLOCK	WISOR, MICHAEL T.
08700129	5664205	150	08/20/1996	POWER MANAGEMENT CONTROL TECHNIQUE FOR TIMER TICK ACTIVITY WITHIN AN INTERRUPT DRIVEN COMPUTER SYSTEM	WISOR, MICHAEL T.
08712867	5862366	150	09/12/1996	SYSTEM AND METHOD FOR SIMULATING A MULTIPROCESSOR ENVIRONMENT FOR TESTING A MULTIPROCESSING INTERRUPT	WISOR, MICHAEL T.

				CONTROLLER	
08727287	5666559	150	10/09/1996	FAIL-SAFE COMMUNICATION ABORT MECHANISM FOR PARALLEL PORTS WITH SELECTABLE NMI OR PARALLEL PORT INTERRUPT	WISOR, MICHAEL T.
08813182	Not Issued	161	03/08/1997	MECHANISM TO SET PROCESSOR SPECIFIC PERFORMANCE RATING INFORMATION	WISOR, MICHAEL T.
08863805	Not Issued	161	05/27/1997	SYSTEM AND METHOD FOR PATCHING MICROCODE DURING THE DEBUGGING OF A PROCESSOR	WISOR, MICHAEL T.
08868797	5815734	150	06/04/1997	A SYSTEM AND METHOD FOR RECONFIGURING CONFIGURATION REGISTERS OF A PCI BUS DEVICE IN RESPONSE TO A CHANGE IN CLOCK SIGNAL FREQUENCY	WISOR, MICHAEL T.
08962361	5974510	250	10/31/1997	METHOD FOR TESTING THE NON-CACHEABLE REGION FUNCTIONING OF A CACHE MEMORY CONTROLLER	WISOR, MICHAEL T.
08974970	6076160	150	11/20/1997	HARDWARE-BASED SYSTEM FOR ENABLING DATA TRANSFERS BETWEEN A CPU AND CHIP SET LOGIC OF A COMPUTER SYSTEM ON BOTH EDGES OF BUS CLOCK SIGNAL	WISOR, MICHAEL T.
08974971	6823435	150	11/20/1997	NON-VOLATILE MEMORY SYSTEM HAVING A PROGRAMMABLY SELECTABLE BOOT CODE SECTION SIZE	WISOR, MICHAEL T.
08976303	5999476	150	11/21/1997	BIOS MEMORY AND MULTIMEDIA DATA STORAGE COMBINATION	WISOR, MICHAEL T.

Inventor Search Completed: No Records to Display.

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